REMARKS

Claim 10 has been cancelled.

Claims 1-9 and 11-16 are pending.

Applicant has amended the title of the specification as suggested by the Examiner. The Abstract also has been amended as required by the Examiner.

Applicant thanks the Examiner for indicating that claims 2, 5, 6, 8, 9, 12, 15 and 16 include allowable subject matter.

The remaining claims were rejected over the prior art as follows:

* Claims 1, 3, 4, 7, 10, 11 and 13 were rejected as anticipated by U.S. Patent No. 6,012,103 (Sartore et al.).

* Claim 14 was rejected as unpatentable over the combination of the Satore et al. patent and U.S. Patent No. 6,000,042 (Henrie).

As discussed below, applicant respectfully requests reconsideration and withdrawal of the claim rejections.

The Sartore et al. patent relates to the use of an USB interface for communications between a host computer and a peripheral device. The Sartore et al. patent discloses that the peripheral device includes a loadable memory (*e.g.*, 174 in FIG. 5) such as RAM or flash EPROM. The peripheral device also may include non-volatile memory (*e.g.*, 178 in FIG. 5), which stores a unique manufacturer identifier (col. 7, lines 43-46). As explained in the following paragraphs, there are patentable distinctions between the disclosure of the Sartore et al. patent and the rejected claims.

Claims 1, 3 and 4

Claim 1 recites that the microcomputer (in contrast to the host) includes two different memories: a nonvolatile memory and a data memory. Those are illustrated respectively, for example, in FIG. 1, as the flash ROM 50 and the RAM 40. Claim 1 recites that program data – received from the host, converted in to parallel data by the USB interface circuit, and stored temporarily in the data memory – is written to a second area of the nonvolatile memory in accordance with a program stored in a first area of the nonvolatile memory. Those features are not disclosed or suggested by the Sartore et al. patent, which discloses only that configuration information (including microprocessor code and configuration data) is downloaded from the host computer to the loadable memory 74 via the USB interface circuit 76. There is no explanation of how or where that configuration data is stored in the loadable memory.

The Office action refers to the memory 64 and operating system 65 (FIG. 2 of the Sartore et al. patent) as somehow corresponding to the claimed non-volatile memory. That is incorrect. First, those components are part of the host computer, not the peripheral device. The Office action improperly selects some components from the host computer, while selecting other components from the peripheral device, and improperly combines them in an attempt to obtain the claimed subject matter.

Nor would there have been any motivation to make the memory 64 and operating system 65 part of the peripheral device. Indeed, the advantage of the system disclosed in the Sartore et al. patent is precisely because those features are located in the host computer and not in the non-volatile memory in the peripheral device (col. 5, lines 2-6).

Therefore, the Sartore et al. patent fails to disclose (or suggest) each and every limitation of claim 1. Claims 3 and 4 should be allowable for at least the same reasons.

Claim 7

Claim 7 recites a temporary register in the USB interface circuit. The register is shown, for example, as item 31 in FIG. 1. The Office action does not identify what feature in the Sartore et al. patent might correspond to the claimed register, and we find none. FIGS. 3 and 4 of the Sartore et al. patent illustrate USB interface circuits, but neither circuit includes a register to store data.

Claims 10 and 11

Independent claim 10 has been cancelled. Therefore, the rejection of that claim is moot. Claim 11 has been rewritten in independent form to include the limitations of claim 10.

Dependent claim 11 recites that program data is written to a second area of the nonvolatile memory in the microcomputer in accordance with a write control program stored in a first area of the nonvolatile memory. As discussed above, that feature is neither disclosed nor suggested by the Sartore et al. patent. Instead, that patent simply discloses that the configuration information (microprocessor code and configuration data) is downloaded over the USB from the host's operating system to the peripheral device's loadable memory. There is no explanation of how or where that configuration data is stored in the loadable memory. Therefore, for reasons similar to those discussed above in connection with claim 1, claim 10 also should be allowed.

Claim 13 and 14

Claim 13 recites a method that includes executing a write control program (stored in nonvolatile memory in the microcomputer) in response to resetting the micro-computer (*see, e.g.*, FIGS. 7 and 9). That is not disclosed by the Sartore et al. patent.

The Office action points to col. 3, lines 18-24 as allegedly disclosing the foregoing feature. That is incorrect. Instead, that section of the patent simply indicates the result of downloading the configuration information from the host to the peripheral device is that the

configuration of the peripheral device is reset from a first configuration to a second configuration. There is no suggestion that a write control program is executed in response to such resetting.

Nor does the Henrie patent disclose that feature. That patent simply illustrates a reset chip 17 connected to the USB controller 10. There is no explanation of what occurs when the USB controller is reset, and there is no suggestion of executing a write control program in response to resetting the controller.

Therefore, claim 13, as well as dependent claim 14, should be allowable.

Conclusion

Applicant respectfully requests allowance of all pending claims.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date:_____

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